ABSTRACT OF THE DISCLOSURE

A semiconductor memory device according to the present invention includes a BIST circuit for evaluating quality of each of memory cells and a buffer (memory) for storing address information of abnormal cells which information is sent from the BIST circuit, the BIST circuit and the buffer being mounted on the same chip as a DRAM. A repair search circuit determines a minimum of address information required to determine redundant cells for replacement in the address information of the abnormal cells which information is sent from the BIST circuit, and stores only the determined address information in the buffer. Since only a minimum of address pairs required determining the redundant cells for repairing the abnormal cells are stored in the buffer, circuit scale is reduced. Further, processing for calculating address information of the redundant cells for repairing the abnormal cells can be performed at high speed.